THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TERUO NAKAGAWA

Appeal No. 95-3889
Application 08/070,296[1]

HEARD: November 3, 1998

Before URYNOWICZ, THOMAS, and FLEMING, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

Decision on Appeal

This appeal is from the final rejection of claims 1-3 and 5-11, all of the claims pending in the application.

The invention pertains to a sequence operation processor and method. Claim 1 is illustrative and reads as follows:

1. A sequence operation processing apparatus for executing operation instructions, said processing apparatus comprising:

[1] Application for patent filed June 2, 1993.

a multi-port RAM for storing data used during execution of the operation instructions;

a sequence operation processor, coupled to said multi-port RAM, for executing the operation instructions, said sequence operation processor including a comparator for comparing a first designated address of said multi-port RAM in a first operation instruction with a second designated address of said multi-port RAM in a second, subsequent operation instruction, and for generating a comparison signal indicating a result of said comparison, the second designated address of said multi-port RAM being read in response to said generated comparison signal indicating that said first and second designated addresses are not equal to each other, wherein said sequence operation processor simultaneously writes data to the first designated address of the multi-port RAM and reads data from the second designated address of the multi-port RAM when said generated comparison signal indicates that said first and second designated addresses are not equal to each other.

The references relied upon by the examiner as evidence of obviousness are:

Loo 4,639,866 Jan. 27, 1987

Runaldue 5,062,081 Oct. 29, 1991

Appellant’s prior art admissions on pages 1-5 of the specification.

Claims 1-3, 5 and 6 stand rejected under 35 U.S.C. § 102(b) as anticipated by Loo.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103 as unpatentable over Loo in view of appellant’s prior art admissions on pages 1-5 of the specification.

Claims 7 and 8 stand rejected under 35 U.S.C. § 103 as unpatentable over Loo in view of Runaldue.

Claim 11 stands rejected under 35 U.S.C. § 103 as unpatentable over Loo in view of Runaldue and appellant’s prior art admissions on pages 1-5 of the specification.

The respective positions of the examiner and the appellant with regard to the propriety of these rejections are set forth in the final rejection (Paper No. 7) and the examiner's answer (Paper No. 14) and the appellant's brief (Paper No. 13) and reply brief (Paper No. 15).

The Rejection of Claims 1-3, 5 and 6

under 35 U.S.C. § 102

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection should not be sustained. Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention. In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657

(Fed. Cir. 1990). With respect to independent claims 1 and 6, appellant is correct that Loo does not disclose a multi-port RAM. With respect to the invention of Loo, at column 4, lines 39-42, it is disclosed that RAM memory 14 acts as a three-port memory. At column 1, lines 54-56, under SUMMARY OF THE INVENTION, Loo refers to his memory as a single-port memory. The fact that Loo's single-port RAM can be made to act like a multi-port RAM does not make it a multi-port RAM. Structurally, it is still a single-port RAM.

Still further with respect to claims 1 and 6, appellant is correct that Loo does not disclose simultaneous read and write operations (claim 1) or that such operations occur at the same time (claim 6). Although phases of instructions N, N+1 and N+2 overlap and are simultaneous, as illustrated in Figure 3 of Loo, and each phase includes both read and write functions, at any given time Loo is performing simultaneous write operations or simultaneous read operations. There are no simultaneous read and write operations. This is illustrated by the figure attached to appellant's reply brief, which figure we acknowledge as an accurate representation of a combination of Loo's Figures 3 and 4. The attached figure shows that the read and write operations to the RAM occur at different times.

Because independent claim 1 is not anticipated by Loo, claims 2, 3 and 5, which depend therefrom, are not anticipated by Loo.

The Rejection of Claims 9 and 10

under 35 U.S.C. § 103

Because claims 9 and 10 depend from claims 5 and 6, respectively, and appellant's prior art admissions on pages 1-5 of the specification have not been shown to include the deficiencies of Loo discussed above, the rejection of these claims will not be sustained.

The Rejection of Claims 7, 8 and 11

Under 35 U.S.C. § 103

In his rejection of these claims, the examiner has not shown that the combined prior art applied against the claims includes the claim requirements of 1.) "a data register for holding data written to said at least one multi-port RAM;" and 2.) that "one of data read from the at least one multi-port RAM and a content of said data register is selected and input to an operation circuit in accordance with the address match signal from said address comparator and the data register valid signal at the same time a data is stored in said at least one multi-port RAM." Nor has it

been shown that the above would have involved obvious modifications of the combined prior art.

Such being the case, a prima facie case of obviousness has not been established, and we will not sustain the rejection of claims 7, 8 and 11. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

REVERSED

STANLEY M. URYNOWICZ)
Administrative Patent Judge)

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JAMES D. THOMAS	)	BOARD OF PATENT
Administrative Patent Judge	)	
	)	APPEALS AND
	)	
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MICHAEL R. FLEMING	)	
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